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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named
Inventor : Ian M. Flanagan et al.

Appln. No. : 09/879,416

Filed : June 12, 2001

For : DELAY-LOCKED LOOP WITH
BUILT-IN SELF-TEST OF PHASE
MARGIN

Docket No.: L13.12-0157/01-191

Group Art Unit

Examiner:

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INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, D.C. 20231

I HEREBY CERTIFY THAT THIS PAPER IS BEING
SENT BY U.S. MAIL, FIRST CLASS, TO THE
ASSISTANT COMMISSIONER FOR PATENTS,
WASHINGTON, D.C. 20231, THIS

12 DAY OF October, 2001.

D. D. R.

PATENT ATTORNEY

Sir:

The patents or publications listed on the enclosed PTO
Form-1449 are submitted pursuant to 37 C.F.R. § 1.97. Copies of
the patents or publications cited are enclosed.

TIME OF FILING

The information disclosure statement is being filed:

1. X with the application or within three months of the
filing date of the application or date of entry into
the national stage of an international application or
before the mailing date of a first Office action on
the merits, whichever event occurs last. In
accordance with 37 C.F.R. § 1.97(b), no statement or
fee is required.

METHOD OF PAYMENT

- X No fee is required.
 Attached is a check in the amount of \$_____.


The Director is authorized to charge any fee deficiency required by this paper or credit any overpayment to Deposit Account No. 12-2252. A duplicate copy of this communication is enclosed.

Respectfully submitted,

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FORM PTO-1449		Atty. Docket No.: L13.12-0157/01-191	Appl. No.: 09/879,416
 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT		First Named Inventor:	
		Ian M. Flanagan et al.	
		Filing Date	Group Art:
		June 12, 2001	

U.S. PATENT DOCUMENTS

Examiner Initial	Document No.	Date	Name	Class	Sub Class	Filing Date If Appropriate
AA						
AB						
AC						
AD						
AE						
AF						
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AH						

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FOREIGN PATENT DOCUMENTS

	Document No.	Date	Country	Class	Sub Class	Translation Yes No
AL						
AM						
AN						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

AO	F.M. Gardner, "Charge-Pump Phase-Lock Loops", IEEE Transactions on Communications, Vol COM-28, No. 11, November 1980, pp. 1849-58.
AP	W.F. Egan, "Phase Lock Basics", Wiley Interscience Publications, New York, 1998, pp. 90-91.
AQ	P.V. Brennan, "Phase Locked Loops: Principles and Practice", McGraw-Hill, New York, 1996, p. 35.
AR	D.H. Wolaver, "Phase-Locked Loop Circuit Design", PTR Prentice Hall, New Jersey, 1991, pp. ix-x.

EXAMINER:

DATE CONSIDERED:

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.